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# Description

# [GOLD BUMP STRUCTURE AND FABRICATING METHOD THEREOF]

## Cross Reference to Related Applications

[0001] This application claims the priority benefit of Taiwan application serial no. 92106257, filed on March 21, 2003.

## Background of Invention

[0002] Field of the Invention

[0003] The present invention relates to a bump structure and a fabricating method thereof, and more particularly to a gold bump structure and a fabricating method thereof.

[0004] Description of the Related Art

[0005] Because of the advance of semiconductor technology, electronic devices also change thereby. During forming electronic devices, the process usually includes: the formation of semiconductor substrate, the formation of semiconductor devices and package process. As to the package process, the flip-chip package process has grad-

ually replaced the traditional package method. Because of the reduction of the signal transmission distance between the chip and substrate, the flip-chip package process has been widely used for packages of high speed devices, such as RF devices. Moreover, the process can also shrink the package size. Accordingly, it also is the most popular package technology in the near future. Generally, the flip-chip package has been applied to for example, high-speed computers, PCMCIA cards, military equipment, personal communication devices, liquid crystal displays, etc.

[0006] The bumps of the package process serve for signal connection between chips and substrates. Metal bumps, such as gold bumps, eutectic solder bumps and high lead solder bumps, have been used for the package of small devices. The gold bumps are most widely used because of their low resistance. However, because of the formation of Au-Sn composition resulting from the rapid interaction of the gold bumps and the solder, too much Au-Sn composition is formed thereat. FIG. 1 is a schematic cross-sectional figure showing a prior art flip-chip gold bump structure.

[0007] Referring to FIG. 1, a gold bump 102 is formed on a chip 100. When the gold bump 102 contacts a solder 104, a

fragile Au-Sn cold joint 106 is formed at the interface thereof, which results in the reliability issue of the package. Therefore, how to prevent the rapid interaction of the gold bump and the solder is a big challenge for the gold bump application therein.

## SUMMARY OF INVENTION

[0008] Therefore, an object of the present invention is to provide a flip-chip gold bump structure and a fabricating method thereof for avoiding the formation of fragile Au-Sn composition resulting from the rapid interaction Au and the solder.

[0009] Another object of the present invention is to provide a flip-chip gold bump structure and a fabricating method thereof for reducing manufacturing costs and simplifying the process thereof.

[0010] The other object of the present invention is to provide a flip-chip gold bump structure and a fabricating method thereof for avoiding generating a fragile soldering point at the interface of the gold bump and the solder.

[0011] According to the objects mentioned above, the present invention discloses a flip-chip gold bump structure formed on a wafer, which comprises: a plurality of gold bumps, a nickel layer and a copper layer, wherein the

nickel layer is formed on the gold bump and the copper layer is formed on the nickel layer for forming a Ni/Cu barrier layer.

[0012] The present invention also discloses a method of fabricating a flip-chip gold bump structure formed on a wafer, which comprises: forming at least one gold bump on the wafer; forming a nickel layer on the gold bump; and forming a copper layer on the nickel layer.

[0013] The present invention also discloses a flip-chip package structure adapted to connect a chip and a chip substrate, which comprises: a plurality of gold bumps, a nickel layer and a solder containing copper, wherein the nickel layer is formed on the gold bump and the solder containing copper is formed on the nickel layer for connecting the chip and the chip substrate.

[0014] The present invention further discloses a method of fabricating a flip-chip package structure adapted to connect a chip and a chip substrate, which comprises: forming at least one gold bump on a wafer; forming a nickel layer on the gold bump; sawing the wafer; forming a solder containing copper on the chip substrate; aligning the gold bump to the solder containing copper; and performing a reflow process.

[0015] The present invention uses a Ni/Cu layer on the gold bump for forming Cu-Ni-Sn composition at the interface of the gold bump structure and the solder instead of the traditional $AuSn_4$ composition. Therefore, the present invention can resolve the issue deriving from the rapid interaction of gold bump structure and the solder.

[0016] In order to make the aforementioned and other objects, features and advantages of the present invention understandable, a preferred embodiment accompanied with figures is described in detail below.

## Brief Description of Drawings

[0017] FIG. 1 is a schematic cross-sectional figure showing a prior art flip-chip gold bump structure.

[0018] FIG. 2 is a schematic cross-sectional view showing a first exemplary gold bump structure of the present invention.

[0019] FIG. 3 is a schematic process flow showing the method of fabricating the flip-chip gold bump structure of FIG. 2.

[0020] FIG. 4 is a schematic cross-sectional view showing a second exemplary flip-chip package of the present invention.

[0021] FIG. 5 is a schematic process flow showing the method of fabricating the flip-chip package of FIG. 4.

## Detailed Description

[0022] FIG. 2 is a schematic cross-sectional view showing a first exemplary gold bump structure of the present invention.

[0023] Referring to FIG. 2, the flip-chip gold bump structure of the present invention formed on a wafer 200, which comprises: gold bumps 202, a nickel layer 204 and the copper layer 206, wherein the gold bump has a height about from 3 μm to about 150 μm. The nickel layer 204 is formed on the gold bump 202 and has a thickness about from 0.1 μm to about 20 μm. The copper layer 206 is formed on the nickel layer 204 and has a thickness about from 0.1 μm to about 10 μm.

[0024] FIG. 3 is a schematic process flow showing the method of fabricating the flip-chip gold bump structure of FIG. 2. Referring to FIG. 3, in step 300, the step of forming the gold bump on the wafer includes electroplating or electroless plating. In step 302, the step of forming the nickel layer on the gold bump includes electroplating or electroless plating. In step 304, the step of forming the copper layer on the nickel layer includes electroplating or electroless plating.

[0025] When the flip-chip gold bump structure of the present invention is applied to the flip-chip package, because of the formation of the Ni/Cu barrier layer on the gold bump,

$AuSn_4$ composition generated from the rapid interaction between Au and Sn can be substantially reduced and Cu-Ni-Sn composition is the prior producthaving a slow growth rate is generated thereat. Therefore, the present invention can resolve the issue resulting from the rapid interaction between the flip-chip gold bump structure and the solder.

[0026] FIG. 4 is a schematic cross-sectional view showing a second exemplary flip-chip package of the present invention.

[0027] The flip-chip package of the present invention formed between a chip 400 and a chip substrate 410, which comprises: gold bumps 402, a nickel layer 404 and a solder containing copper 406, wherein the gold bump has a height about from 3 μm to about 150 μm and the solder containing copper can be a solder alloy and have copper from about 0.7 wt.% to about 3.0 wt.%. The nickel layer 404 is formed on the gold bump 402 and has a thickness about from 0.1 μm to about 20 μm. The solder containing copper 406 is formed on the chip substrate 410 for connecting the chip 400 and chip substrate 410.

[0028] FIG. 5 is a schematic process flow showing the method of fabricating the flip-chip package of FIG. 4. Referring to FIG. 5, in step 500, the step of forming the gold bump on

the wafer includes electroplating or electroless plating. In step 502, the step of forming the nickel layer on the gold bump includes electroplating or electroless plating. In step 504, the wafer is sawed into several dies. In step 506, the solder containing copper, which can be a solder alloy and have copper from about 0.7 wt.% to about 3.0 wt.% is formed on the chip substrate. In step 508, the gold bump is aligned to the solder containing copper for connecting thereof. In step 510, a reflow process is performed.

[0029] When the present invention is applied to the flip-chip package, Cu-Ni-Sncomposition is formed at the interface of the gold bump structure and the solder during the reflow process instead of the traditional $AuSn_4$ composition. Therefore, the present invention can resolve the issue deriving from the rapid interaction of gold bump structure and the solder.

[0030] Although the present invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be constructed broadly to include other variants and embodiments of the invention which may be made by those skilled in the field of this art without departing from the

scope and range of equivalents of the invention.